REMARKS

Claims 1-13 are pending in this application. Claims 1-13 stand rejected. The Examiner's reconsideration of the rejection is respectfully requested in view of the following remarks.

Rejections Under 35 U.S.C. § 102:

Claims 1-4, 7, 10 and 12-13 stand rejected under 35 U.S.C § 102(e) as being anticipated by U.S. Patent No. 6,730,950 to Seshadri for the reasons stated on pages 2-4 of the Final Office Action.

Applicant respectfully submits that at the very least Seshadri does not anticipate claim 1. In fact, as will be explained hereafter, the Examiner has erroneously interpreted the teachings of Seshadri, and improperly fit the claim language to such erroneous interpretation to support the rejection. For instance, Seshadri does not disclose or suggest "*a MOS transistor having a floating gate electrode*," as essentially recited in claim 1. Examiner contends on page 2 of the Final Office Action that Seshadri discloses a MOS transistor having a floating gate electrode in Figs. 5C, 6B and 10C. However, it is respectfully submitted that the Examiner's interpretation of Seshadri is wrong because the MOS transistor does not have a floating gate.

One of ordinary skill in the art readily understands that a floating gate electrode is a gate element that is electrically insulated and stores an electrical charge. In contrast, in Fig. 5C, the gate (69c) of MOS transistor is electrically connected to other circuit elements such as drain/source regions (69b) via the bottom plate (67) of the capacitor which forms a local interconnect layer (61) for electrically coupling a plurality of elements E1-EN through contacts (61a, 61b, 61c, 61d). (See Col. 9 lines 40-66). Moreover, in Fig. 6B, the gate (79c) of MOS

transistor (94) is not a floating gate, but rather the gate (79c) is connected to drain/source regions (79b) of other transistor elements (92) via the bottom plate (77) of the capacitor as a local interconnect layer for electrically coupling the gate of transistor (94) via contacts (71a, 71b, 71c) as schematically depicted in Fig. 6A. Furthermore, with respect to Fig. 10C, the same argument as above applies. Therefore, based on the above, there is simply no basis for Examiner's interpretation of Seshadri as disclosing a floating gate.

Furthermore, in view of the above, the remaining anticipation analysis is fundamentally flawed. For instance, Seshadri does not disclose or suggest "*a floating gate electrode, a floating gate plug, and a lower electrode constituting a conductive structure which is electrically insulated*", as essentially recited in claim 1. To begin, as explained above, Seshadri does not disclose a floating gate.

Moreover, Examiner's contention on page 6 of the Final Office Action that "the claimed language does not specifically state what the conductive structure is electrically insulated from" is based on a strained interpretation of the claim language and misses the point. In Fig. 5C, the conductive structure including a gate electrode (69c), a gate plug (61c), and a lower electrode (61) does not constitute a conductive structure which is electrically insulated – indeed, the lower electrode (61) is electrically connected to other circuit elements such as a drain region (69b) through gate plugs (61b and 61d) in E2 and E4 regions. (See Figs. 5C). In contrast, as claimed in claim 1, the structure that is constituted by a floating gate electrode, a floating gate plug, a lower electrode is a conductive structure that is electrically insulated. Based on a reasonable interpretation of the claim language of claim 1 in view of the specification, it is clear that the conductive structure constituting a floating gate electrode, a floating gate plug, and a lower electrode is insulated from all surrounding components.

Therefore, the Applicant respectfully submits that claim 1 is not anticipated by Seshadri. Claims 2-4, 7, 10, 12 and 13 depend from claim 1 which, for the reasons stated hereinabove, is submitted not to be anticipated by the cited reference.

Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 2-4, 7, 10, 12 and 13 under 35 U.S.C § 102(e) and that claims 1, 2-4, 7, 10, 12 and 13 are in condition for allowance.

Rejections Under 35 U.S.C. § 103:

Claims 5 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Seshadri for the reasons stated on pages 4 to 5 of the Final Office Action. Claims 5 and 11 depend from claim 1. These dependent claims are believed to be patentable over Seshadri at least for the same reasons given for claim 1. Accordingly, withdrawal of the obviousness rejections is respectfully requested.

Claims 6, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Seshadri in view of U.S. Patent No. 6,602,749 to Tu for the reasons stated on pages 5 to 6 of the Final Office Action. Claims 6, 8 and 9 depend from claim 1. These dependent claims are believed to be patentable over Seshadri in view of Tu at least for the same reasons given for claim 1. Further, the addition of Tu does not render the claimed features obvious because Tu discloses neither "a MOS transistor having a floating gate" nor "a floating gate electrode, a floating gate plug, and a lower electrode constituting a conductive structure which is electrically insulated", as essentially recited in claim 1. Accordingly, withdrawal of the obviousness rejections is respectfully requested.

For the foregoing regions, the present invention, including claims 1-13, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully requested. The Examiner is invited to contact the undersigned if he has any questions or comments in this matter.

Respectfully submitted,

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